

FIG. 3

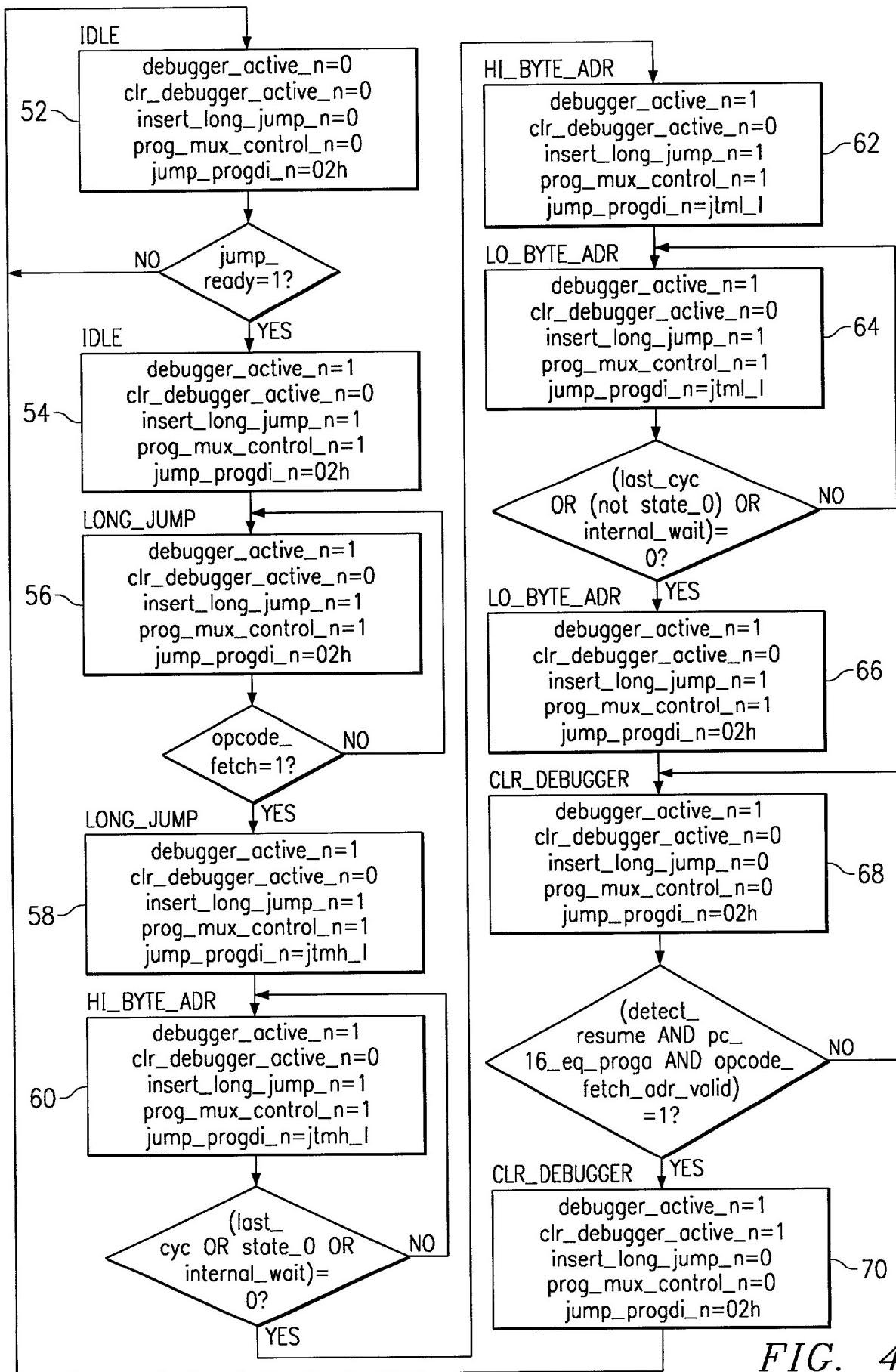


FIG. 4

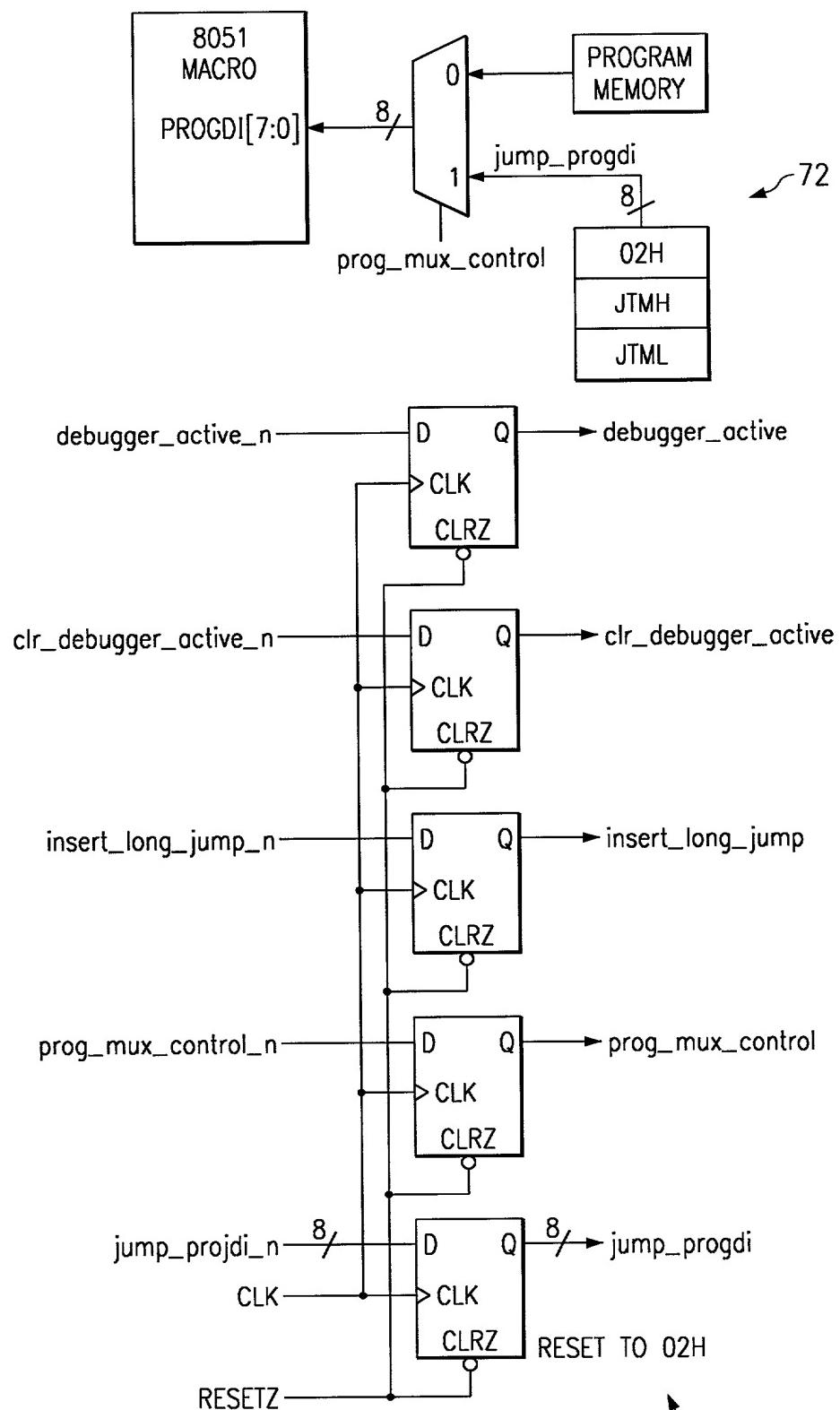
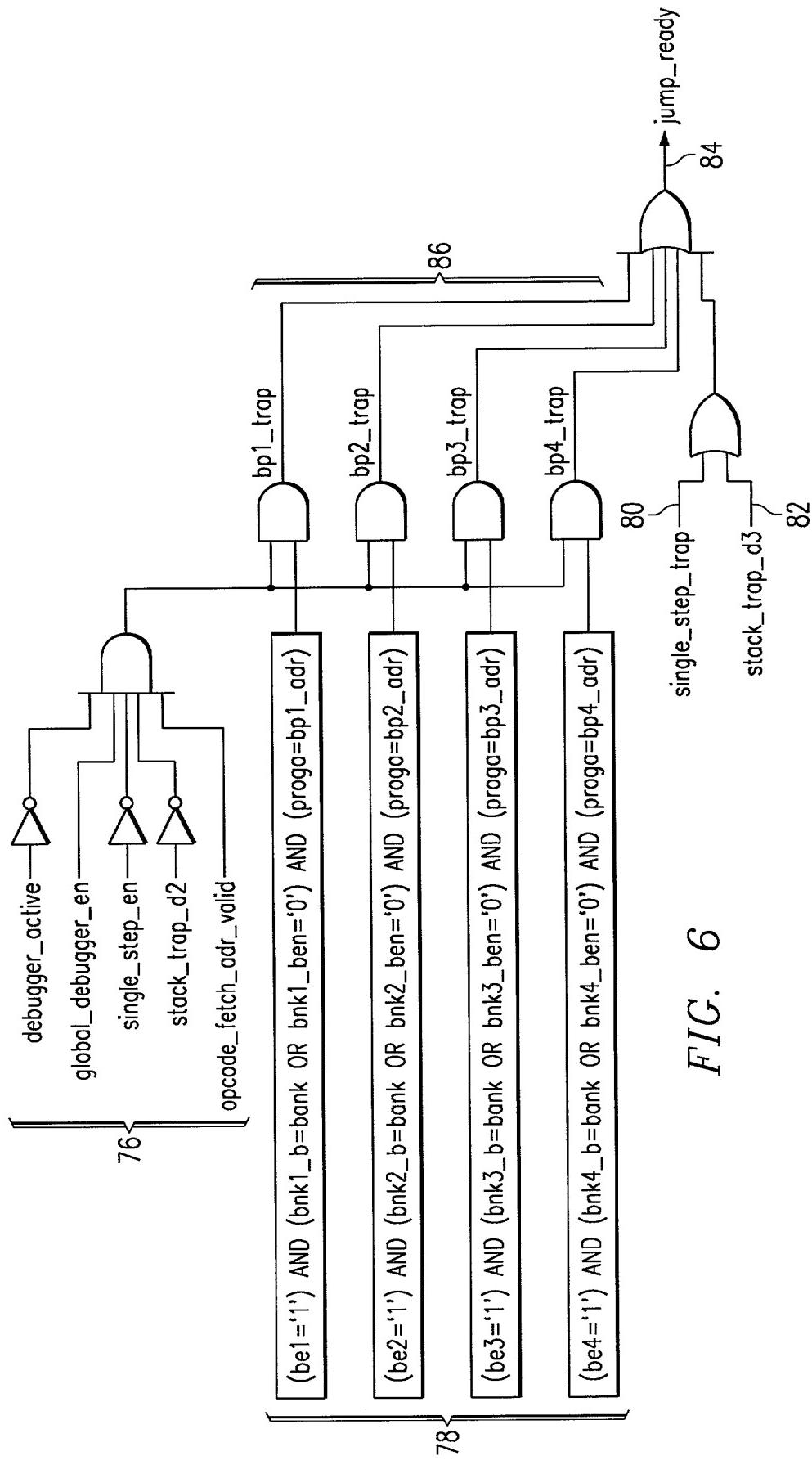


FIG. 5



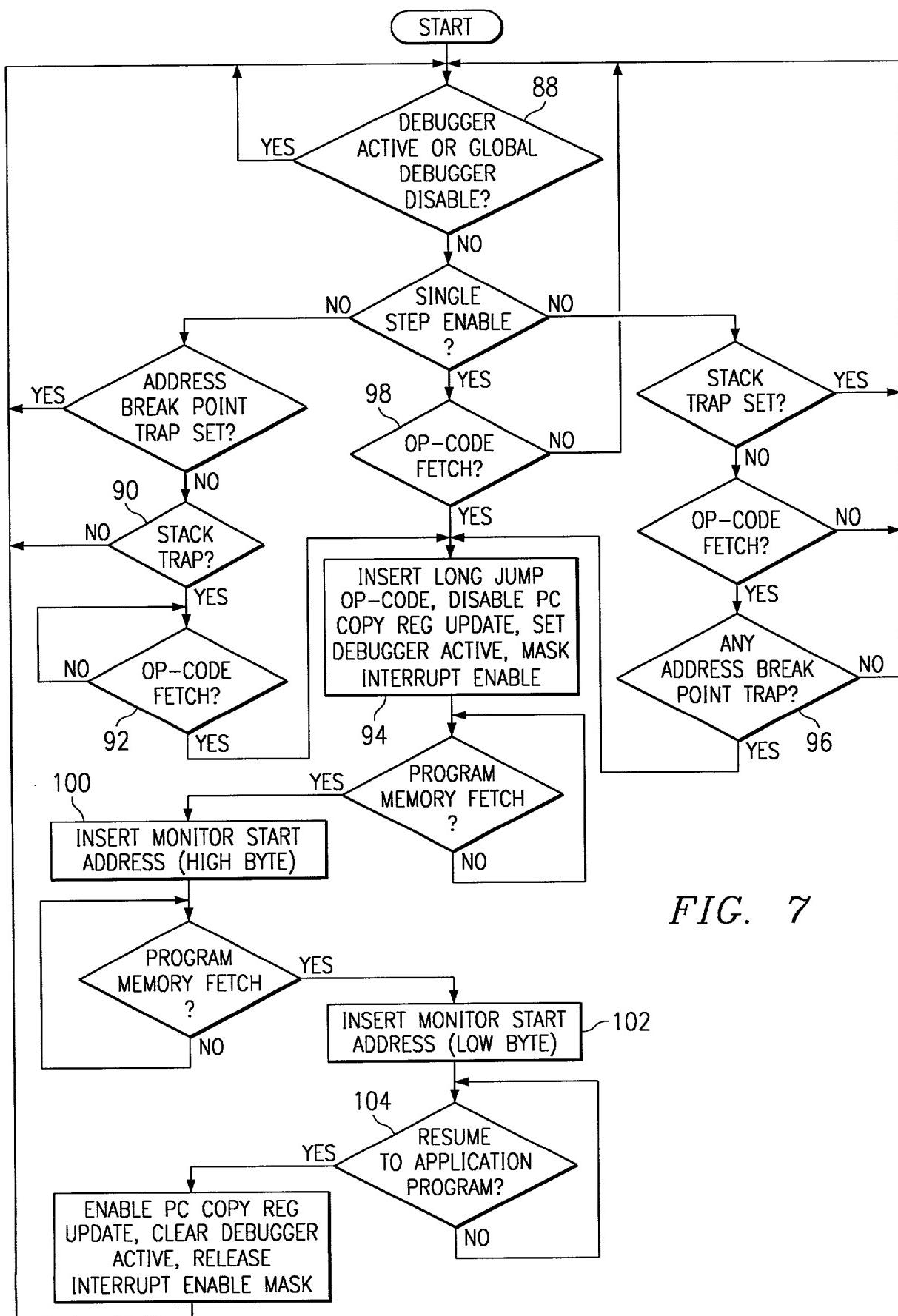


FIG. 7

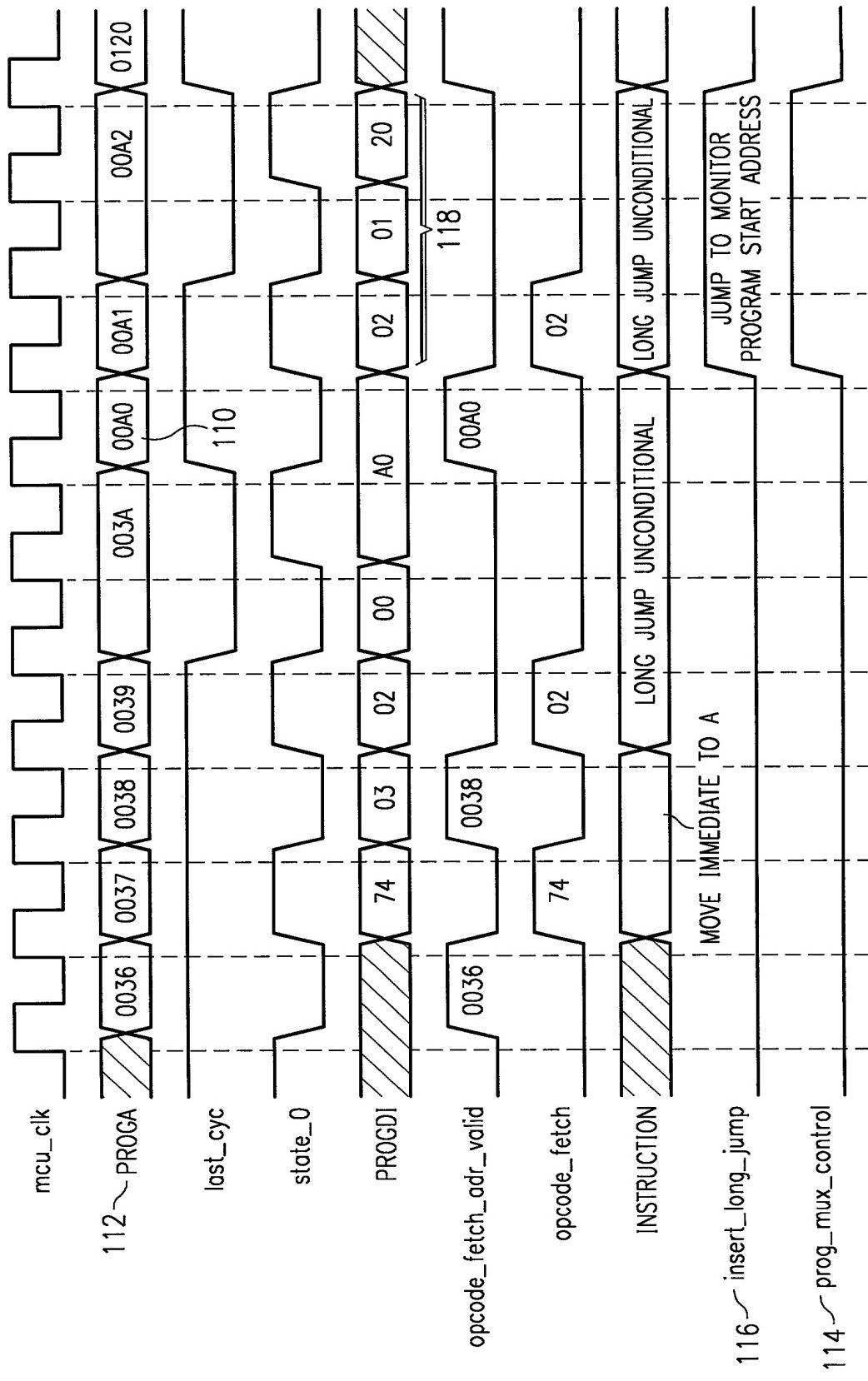


FIG. 8a

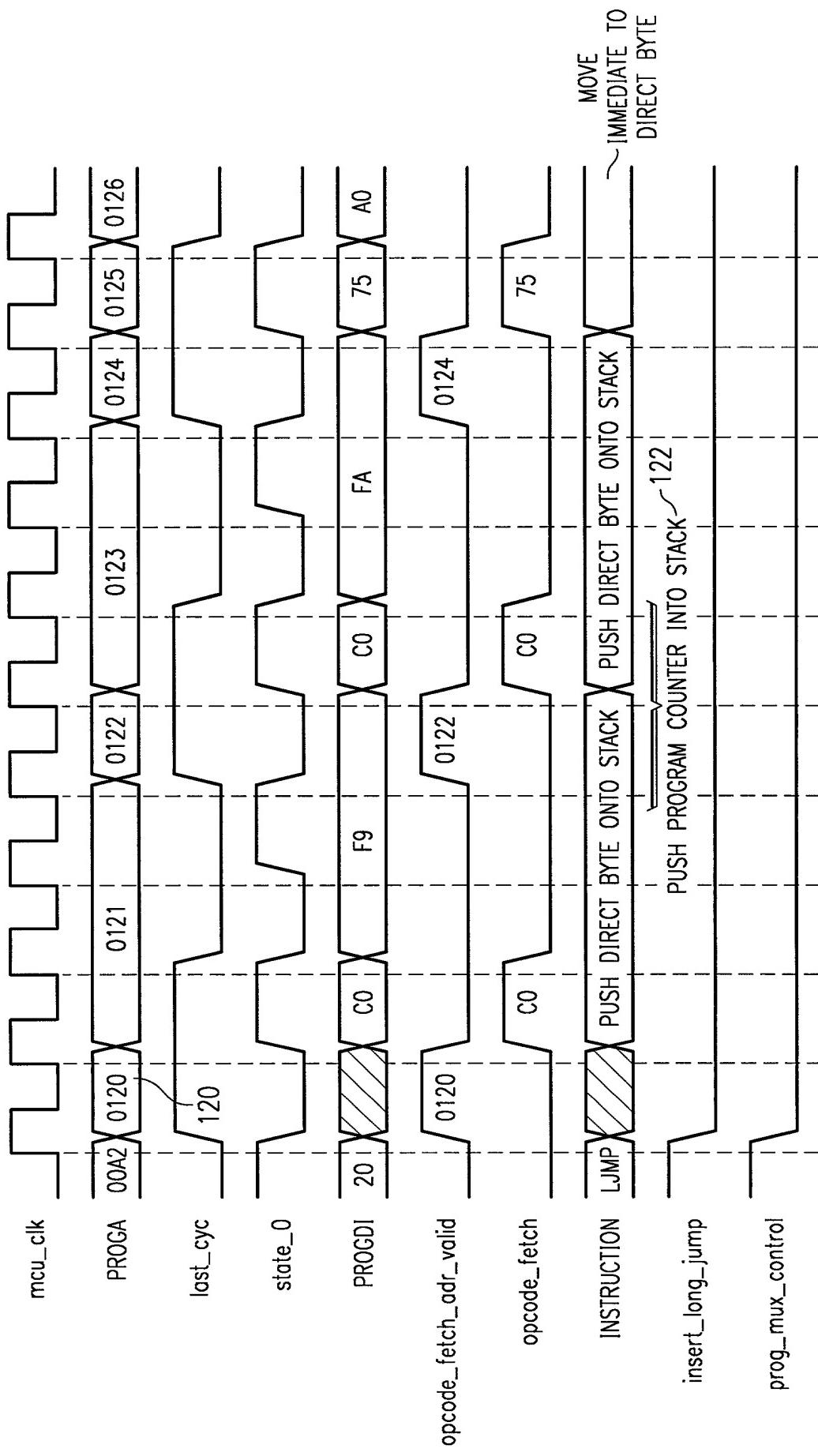


FIG. 8b

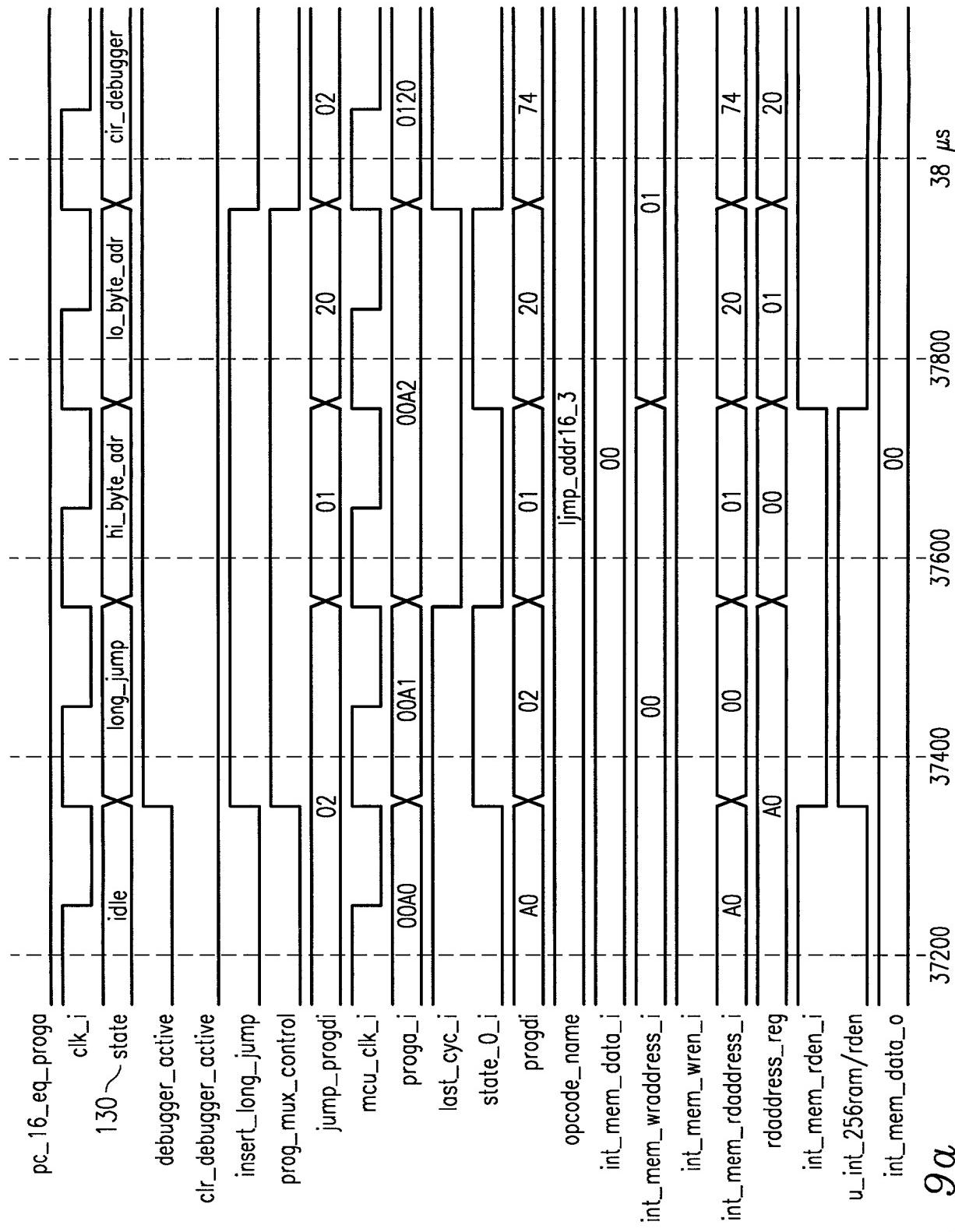


FIG. 9a

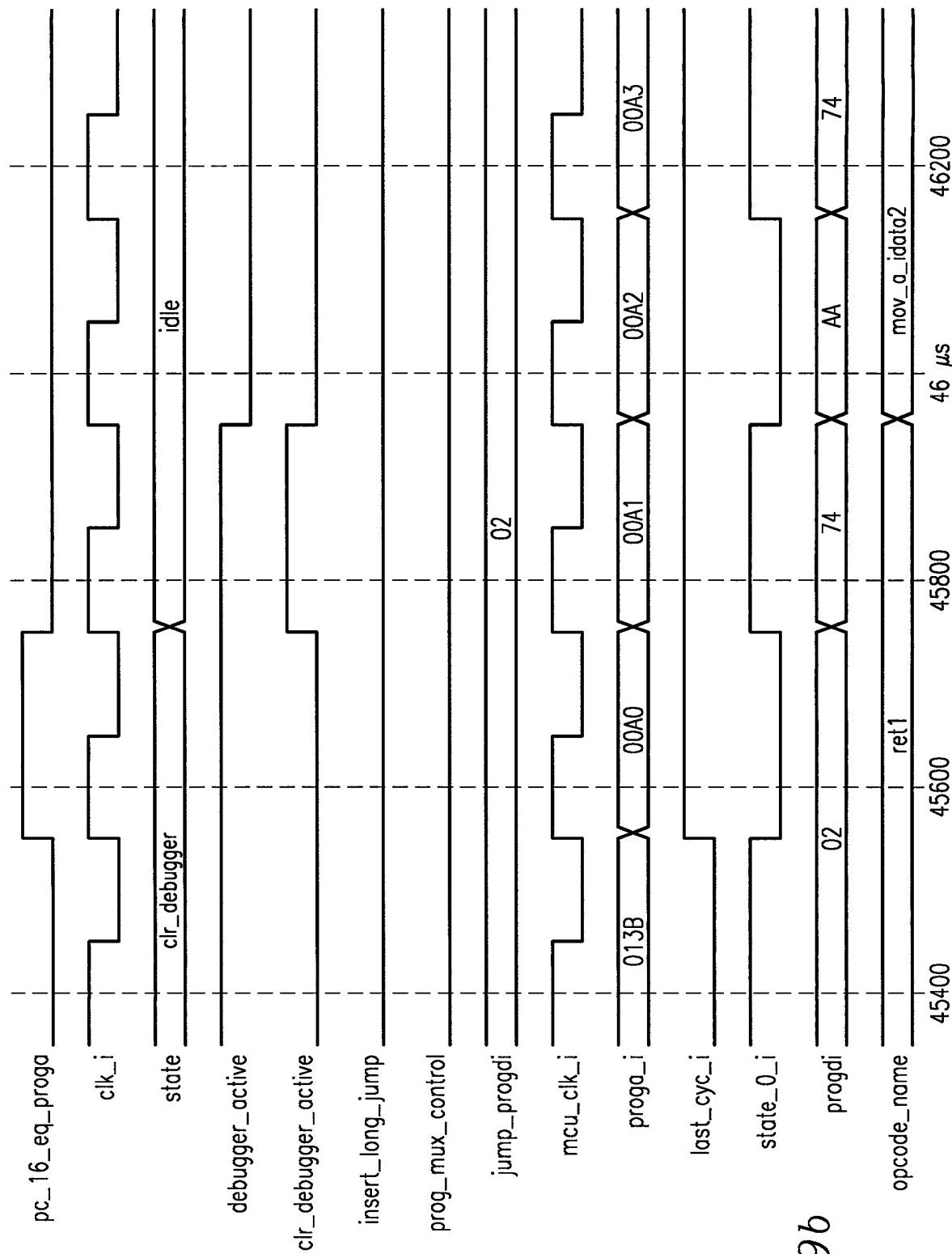


FIG. 9b

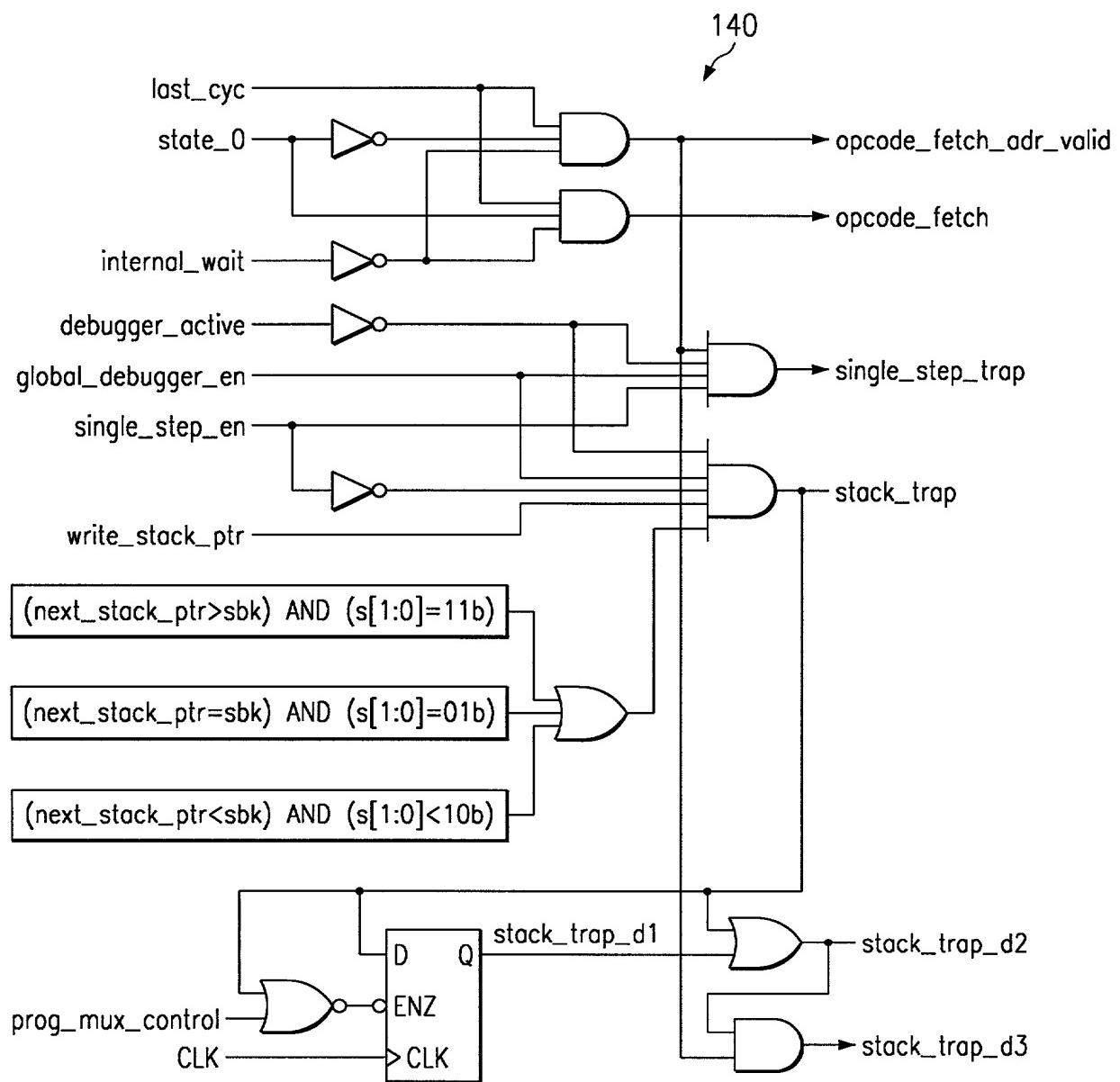


FIG. 10

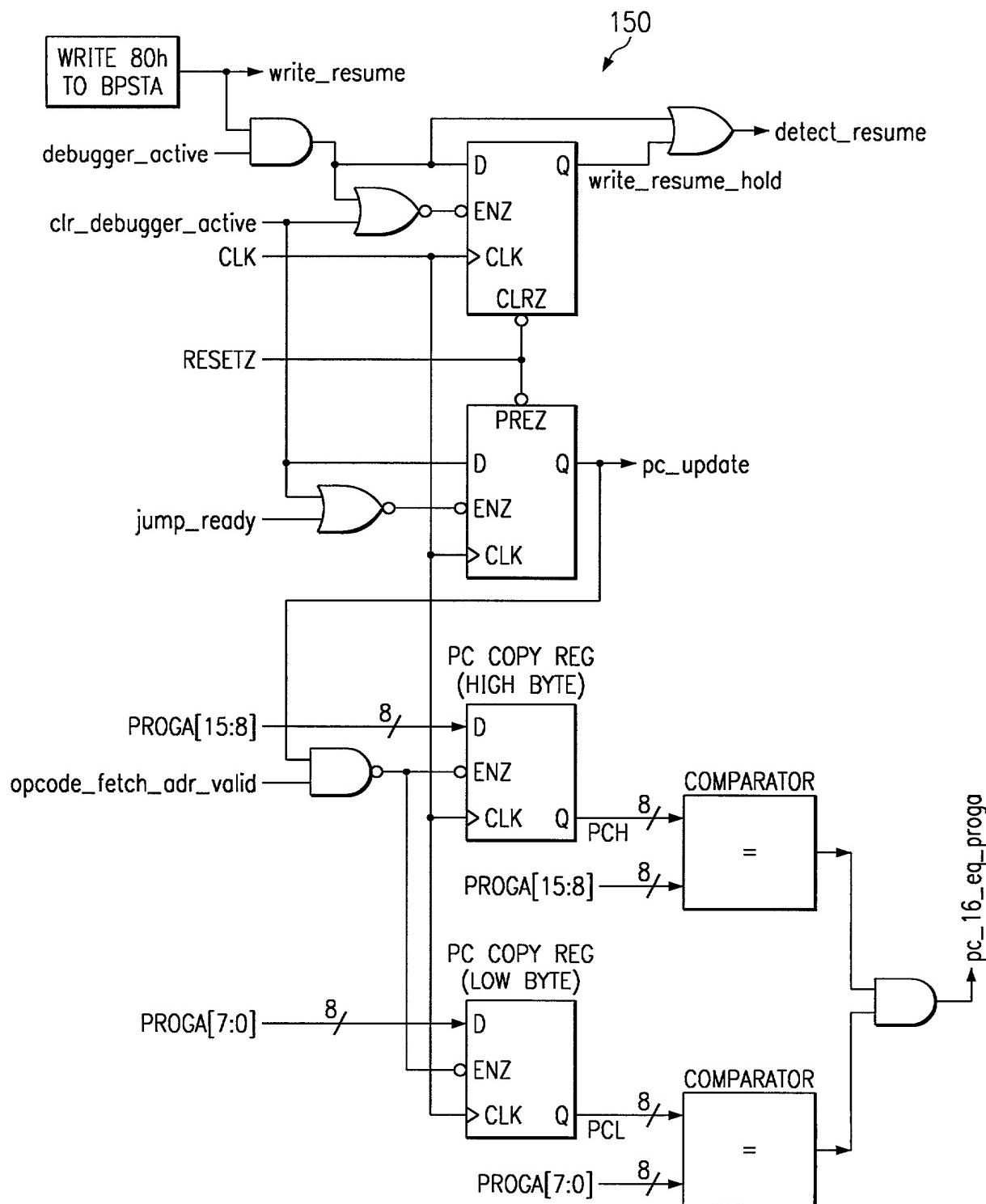


FIG. 11

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FIG. 12

DESCRIPTION	LABEL	ADDRESS
PORT-0	P0	80
162 } STACK POINTER	SP	81
DATA POINTER LB	DPL	82
DATA POINTER HB	DPH	83
POWER CONTROL REG	PCON	87
TIMER/COUNTER CONTROL	TCON	88
TIMER/COUNTER MODE	TMOD	89
TIMER/COUNTER-0 LB	TLO	8A
TIMER/COUNTER-1 LB	TL1	8B
TIMER/COUNTER-0 HB	TH0	8C
TIMER/COUNTER-1 HB	TH1	8D
PORT-1	P1	90
SERIAL CONTROL REGISTER	SCOM	98
SERIAL DATA BUFFER	SBUF	99
PORT-2	P2	A0
INTERRUPT ENABLE REGISTER	IE	A8
PORT-3	P3	B0
INTERRUPT PRIORITY REGISTER	IP	B8
BPSTA: BREAK POINT STATUS REGISTER	BPSTA	BD
BPL1: BREAK POINT REGISTER-1 (LB)	BPL1	BE
BPH1: BREAK POINT REGISTER-1 (HB)	PBH1	BF
BNK1: BREAK POINT BANK REGISTER-1	BNK1	C0
BPL2: BREAK POINT REGISTER-2 (LB)	BPL2	C1
BPH2: BREAK POINT REGISTER-2 (HB)	PBH2	C2
BNK2: BREAK POINT BANK REGISTER-2	BNK2	C3
BPL3: BREAK POINT REGISTER-3 (LB)	BPL3	C4
BPH3: BREAK POINT REGISTER-3 (HB)	PBH3	C5
BNK3: BREAK POINT BANK REGISTER-3	BNK3	C6
BPL4: BREAK POINT REGISTER-4 (LB)	BPL4	C7
BPH4: BREAK POINT REGISTER-4 (HB)	PBH4	C8
BNK4: BREAK POINT BANK REGISTER-4	BNK4	C9
JTML: JUMP TO MONITOR ADDRESS REGISTER (LB)	JTML	CA
JTMH: JUMP TO MONITOR ADDRESS REGISTER (HB)	JTMH	CB
RESERVED		CC
RESERVED		CD
SBK: STACK BREAK POINT REGISTER	SBK	CE
BPCRL: BREAK POINT CONTROL REGISTER	BPCRL	CF
PROGRAM STATUS WORD	PSW	DO
D1 → DF IS USED FOR SCRATCH PAD		D1 → DF
ACCUMULATOR	A	E0
INTERRUPT ENABLE REGISTER-1	IE1	E8
B REGISTER	B	F0
RTKTM: RTK TIMER REGISTER	RTKT	F6
VECINT: VECTOR INTERRUPT REGISTER	VEC1	F7
INTERRUPT PRIORITY REGISTER-1	IP1	F8
PCL: PC COPY REGISTER (LB)	PCL	F9
PCH: PC COPY REGISTER (HB)	PCH	FA
WDCSR: WATCHDOG TIMER CONTROL AND STATUS REGISTER	WDCR	FB
MCNFG: MCU CONFIGURATION REGISTER	MCNFG	FC
WSCEN: WAIT-STATE GENERATOR REGISTER	WSCEN	FD
DSOVL: DATA-SPACE AND OVERLAY DEFINITION REGISTER	OVLAY	FE
BANK: BANK SELECT REGISTER	BANK	FF

	7	6	5	4	3	2	1	0	
	A7	A6	A5	A4	A3	A2	A1	A0	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
170	BIT	NAME	RESET	FUNCTION					
170	7-0	A[7:0]	00h	SET-1: LOW-BYTE OF BREAK POINT ADDRESS					

	7	6	5	4	3	2	1	0	
	A15	A14	A13	A12	A11	A10	A9	A8	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
172	BIT	NAME	RESET	FUNCTION					
172	7-0	A[15:8]	00h	SET-1: HIGH-BYTE OF BREAK POINT ADDRESS					

	7	6	5	4	3	2	1	0	
	BEN	RSV	RSV	RSV	B3	B2	B1	B0	
	R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W	
174	BIT	NAME	RESET	FUNCTION					
174	3-0	B[3:0]	0h	SET-1 OF BANK, BREAK POINT ADDRESS					
174	6-4	RSV	0h	RESERVED=0					
174	7	BEN	0	BANK, BREAK POINT ENABLE/DISABLE BIT BEN=0 BANK, BREAK POINT ADDRESS IS DISABLED BEN=1 BANK, BREAK POINT ADDRESS IS ENABLED					

FIG. 13

	7	6	5	4	3	2	1	0	
	A7	A6	A5	A4	A3	A2	A1	A0	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
180	BIT	NAME	RESET	FUNCTION					
180	7-0	A[7:0]	00h	LOW-BYTE OF THE JUMP TO MONITOR ADDRESS					

	7	6	5	4	3	2	1	0	
	A15	A14	A13	A12	A11	A10	A9	A8	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
182	BIT	NAME	RESET	FUNCTION					
182	7-0	A[15:8]	00h	HIGH-BYTE OF THE JUMP TO MONITOR ADDRESS					

FIG. 14

	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT	NAME	RESET	FUNCTION					
7-0	A[7:0]	00h	STACK ADDRESS, USED TO COMPARE AGAINST THE STACK. IF A TRAP CONDITION IS DETECTED A LJMP TO MONITOR WILL BE INSERTED.					

FIG. 15

	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
	R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
BIT	NAME	RESET	FUNCTION					
7-0	P[7:0]	00h	LOW BYTE OF THE PC. THIS VALUE IS LATCHED BY THE BREAK POINT LOGIC AND CAN BE READ ONLY BY MCU. MONITOR WILL USE THIS ADDRESS TO RESUME THE APPLICATION.					

	7	6	5	4	3	2	1	0
	P15	P14	P13	P12	P11	P10	P9	P8
	R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
BIT	NAME	RESET	FUNCTION					
7-0	P[7:0]	00h	HIGH BYTE OF THE PC. THIS VALUE IS LATCHED BY THE BREAK POINT LOGIC AND CAN BE READ ONLY BY MCU. MONITOR WILL USE THIS ADDRESS TO RESUME THE APPLICATION.					

FIG. 18

	7	6	5	4	3	2	1	0					
	BPE	STE	S1	S0	BE4	BE3	BE2	BE1					
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					
200	0	0	0	0	0	0	0	0					
BIT	NAME	RESET	FUNCTION										
0	BE1	0	ADDRESS BREAK POINT-1 CONTROL BIT										
			BE1=0 ADDRESS BREAK POINT-1 IS DISABLED										
			BE1=1 ADDRESS BREAK POINT-1 IS ENABLED. IF A MATCH IS DECODED, THE JUMP LOGIC WILL BE TRIGGERED.										
202	1	0	ADDRESS BREAK POINT-2 CONTROL BIT										
			BE2=0 ADDRESS BREAK POINT-2 IS DISABLED										
			BE2=1 ADDRESS BREAK POINT-2 IS ENABLED. IF A MATCH IS DECODED, THE JUMP LOGIC WILL BE TRIGGERED.										
202	2	0	ADDRESS BREAK POINT-3 CONTROL BIT										
			BE3=0 ADDRESS BREAK POINT-3 IS DISABLED										
			BE3=1 ADDRESS BREAK POINT-3 IS ENABLED. IF A MATCH IS DECODED, THE JUMP LOGIC WILL BE TRIGGERED.										
202	3	0	ADDRESS BREAK POINT-4 CONTROL BIT										
			BE4=0 ADDRESS BREAK POINT-4 IS DISABLED										
			BE4=1 ADDRESS BREAK POINT-4 IS ENABLED. IF A MATCH IS DECODED, THE JUMP LOGIC WILL BE TRIGGERED.										
204	5-4	00b	STACK TRAP CONDITION 00b=NO STACK TRAP (STACK TRAP IS DISABLED) 01b=STACK TRAP ON SP=SBK 10b=STACK TRAP ON SP<SBK 11b=STACK TRAP ON SP>SBK										
206	6	0	SINGLE STEP ENABLE/DISABLE CONTROL BIT. SEE SINGLE STEP FOR MORE EXPLANATION. STE=0 SINGLE STEP IS DISABLE STE=1 SINGLE STEP IS ENABLED										
208	7	0	GLOBAL DEBUGGER ENABLE/DISABLE CONTROL BIT										
			BPE=0 THE DEBUGGER LOGIC IS DISABLED. NO BREAK CAN HAPPEN. HOWEVER WRITING TO ALL DEBUGGER REGISTERS IS POSSIBLE.										
			BPE=1 THE DEBUGGER LOGIC IS ENABLED										

FIG. 16

	7	6	5	4	3	2	1	0
	RES	EA	SSP	SB	B4	B3	B2	B1
	W/O	R/O						

FIG. 17

BIT	NAME	RESET	FUNCTION
0	B1	0	ADDRESS BREAK POINT-1 STATUS BIT
			B1=0 ADDRESS BREAK POINT-1 DIDN'T CAUSED A BREAK CONDITION
			B1=1 INDICATES THAT ADDRESS BREAK POINT-1 CAUSED THE BREAK CONDITION. THIS BIT WILL BE CLEARED WHEN MCU WRITE "80h" TO THIS REGISTER.
1	B2	0	ADDRESS BREAK POINT-2 STATUS BIT
			B2=0 ADDRESS BREAK POINT-2 DIDN'T CAUSED A BREAK CONDITION
			B2=1 ADDRESS BREAK POINT-2 CAUSED THE BREAK CONDITION. THIS BIT WILL BE CLEARED WHEN MCU WRITE "80h" TO THIS REGISTER.
2	B3	0	ADDRESS BREAK POINT-3 STATUS BIT
			B3=0 ADDRESS BREAK POINT-3 DIDN'T CAUSED A BREAK CONDITION
			B3=1 ADDRESS BREAK POINT-3 CAUSED THE BREAK CONDITION. THIS BIT WILL BE CLEARED WHEN MCU WRITE "80h" TO THIS REGISTER.
3	B4	0	ADDRESS BREAK POINT-4 STATUS BIT
			B4=0 ADDRESS BREAK POINT-4 DIDN'T CAUSED A BREAK CONDITION
			B4=1 ADDRESS BREAK POINT-4 CAUSED THE BREAK CONDITION. THIS BIT WILL BE CLEARED WHEN MCU WRITE "80h" TO THIS REGISTER.
4	SB	0	STACK TRAP STATUS BIT
			SB=0 STACK TRAP DIDN'T CAUSED A BREAK CONDITION
			SB=1 STACK TRAP CAUSED THE BREAK CONDITION. THIS BIT WILL BE CLEARED WHEN MCU WRITE "80h" TO THIS REGISTER.
5	SSP	0	SINGLE STEP BREAK POINT STATUS BIT
			SSP=0 SINGLE STEP BREAK POINT DIDN'T CAUSED A BREAK CONDITION
			SSP=1 SINGLE STEP BREAK POINT CAUSED THE BREAK CONDITION. THIS BIT WILL BE CLEARED WHEN MCU WRITE "80h" TO THIS REGISTER.
6	EA	0	REFLECTS THE REAL VALUE OF EA BIT WHEN IN DEBUG MODE. SEE SINGLE STEP FOR MORE EXPLANATION.
			EA=0 INTERRUPT IS DISABLED EA=1 INTERRUPT IS ENABLED
218	7	RES	RESUME CONTROL BIT. WRITING A "80h" TO THIS REGISTER WILL WRITE-PROTECT ESFR(BE-CF), ENABLE THE PCL/PCH UPDATE AND CLEAR B[4:1] BITS. THIS BIT IS READ AS "0". WRITING A "55h" TO THIS REGISTER WILL UNPROTECT ESFR(BE-CF) BUT NOT CLEAR THE STATUS BITS.